AMENDMENTS TO THE CLAIMS:

1. (Currently amended): A TFT comprising a polycrystalline silicon channel extending between a source and drain, a gate overlying the channel, and of a thickness to define an upstanding gate side wall, an LDD region, and a spacer overlying the LDD region, wherein the spacer comprises a conductive region that both overlies the LDD region and extends along the upstanding gate side wall thereby forming a corner therebetween, and a fillet formed on the conductive region at the corner.

2. (Currently amended): ~~A~~ The TFT according to claim 1 wherein the conductive region comprises a layer that is thinner than the thickness of the gate and has a first portion overlying the LDD region and a second portion extending along the upstanding side wall of the gate.

3. (Currently amended): ~~A~~ The TFT according to claim 2 wherein the conductive region comprises a layer of conductive material.

4. (Currently amended): ~~A~~ The TFT according to claim 3 wherein the layer is a metallic layer deposited by sputtering.

5. (Currently amended): ~~A~~ The TFT according to claim 3 wherein the layer comprises a doped semiconductor material.

6-7. (Canceled)

8. (Currently amended): A method ~~according to claim 7, wherein step (c) comprises~~ of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate separated from a polycrystalline silicon layer by an insulating layer;

(b) implanting a dopant into the polycrystalline silicon layer using the gate as a mask;

(c) forming a spacer after step (b) adjacent to the gate that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall, comprising depositing a layer of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate, wherein the layer of conductive material has a thickness less than that of the gate; and

(d) implanting a dopant into the polycrystalline silicon layer using the gate and the spacer as a mask to form a source or drain region, such that the spacer overlies an LDD region in the polycrystalline silicon layer between the source or drain region and the channel.

9. (Currently amended): ~~A~~ The method according to claim ~~9~~ 8 including depositing the layer of conductive material to a thickness which is less than that of the gate.

10. (Currently amended): ~~A~~ The method according to claim 8 ~~or 9~~ including depositing the conductive material in a non-conformal layer.

11. (Currently amended): ~~A~~ The method according to claim 8 including depositing the layer by sputtering.

12. (Currently amended): ~~A~~ The method according to claim 8 including depositing said layer as a metallic layer.

13. (Currently amended): A method ~~according to claim 8~~ of fabricating a polycrystalline silicon channel TFT with a gate overlying the channel, having an upstanding gate side wall, the method comprising the steps of:

(a) providing a gate separated from a polycrystalline silicon layer by an insulating layer;

(b) implanting a dopant into the polycrystalline silicon layer using the gate as a mask;

(c) forming a spacer after step (b) adjacent to the gate that comprises a conductive region which overlies the polycrystalline silicon layer and extends along the gate side wall, comprising depositing a layer of conductive material over the polycrystalline silicon layer and the gate, and selectively etching the deposited layer of conductive material to form the spacer with a first portion overlying the polycrystalline silicon layer and a second portion extending along on the side wall of the gate, wherein the selective etching of the conductive layer is carried out by forming a fillet over the first portion thereof, and selectively etching the conductive layer where not protected by the fillet; and

(d) implanting a dopant into the polycrystalline silicon layer using the gate and the spacer as a mask to form a source or drain region, such that the spacer overlies an LDD region in the polycrystalline silicon layer between the source or drain region and the channel.

14. (Currently amended): ~~A~~ The method according to claim 13 ~~11~~ including depositing a further layer on said conductive layer, and selectively etching the further layer to form the fillet therefrom.

15. (Currently amended): ~~A~~ The method according to claim 14 including depositing the further layer as a conformal layer.

16. (Currently amended): ~~A~~ The method according to claim 14 including depositing the further layer as a Si containing layer.

17. (Currently amended): ~~A~~ The method according to claim 14 ~~13~~ including depositing the further layer by CVD[[,]] .

18-19. (Canceled)